

IN THE UNITED STATES PATENT OFFICE

Applicant: Kevin T. Look
Assignee: Xilinx, Inc.
Title: "Low Voltage Non-Volatile Memory Cell"
Serial No.: Not Yet Known File Date: 10-24-03
Examiner: Not Yet Known Art Unit: Not Yet Known

Divisional of
Serial No.: 10/283,736 File Date: 10-29-02
Docket No.: X-719-1D-2D US

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INFORMATION DISCLOSURE STATEMENT

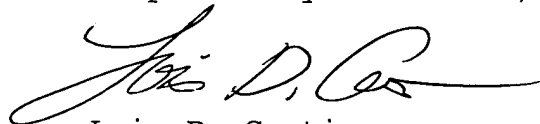
Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant brings to the attention of the Examiner the twenty-two (22) references listed in the attached Substitute for Form PTO-1449 (Information Disclosure Statement by Applicant).

All of these references were cited in prior related U.S. patent application Serial Number 10/283,736 filed October 29, 2002 to which this application claims priority. Copies of these references have not been supplied herein since they were previously submitted in the parent case.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully Submitted,



Lois D. Cartier
Agent for Applicant
Reg. No. 40,941

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	2
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Complete if Known

Application / Conf. No.	Unknown /
Filing Date	October 24, 2003
First Named Inventor	Kevin T. Look
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	X-719-ID-2D US

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ^o
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
		JP 40623289 A	08-01-94	Kou		
		JP 360009160 A	01-18-85	Fukumoto et al.		
		JP 408264660 A	10-11-96	Yamamoto		
		JP 2000077356 A	03-14-00	Sheen		
		JP 406232389 A	08-19-94	Kou		
		JP 363079377 A	04-09-88	Kita		
		JP 406163906 A	06-10-94	Natsume		

Examiner
Signature

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application / Conf. No.	Unknown /
				Filing Date	October 24, 2003
				First Named Inventor	Kevin T. Look
				Art Unit	Unknown
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	X-719-1D-2D US

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		"Boron Diffusion And Penetration In Ultrathin Oxide With Poly-Si Gate"; Cao et al.; IEEE Electron Device Letters; Vol. 19; No. 8; August 1998; pp. 291-293	
		"Flat-band Voltage Shifts In P-MOS Devices Caused By Carrier Activation In P+-Polycrystalline Silicon and Boron Penetration"; Aoyama et al.; 1997 IEEE; pp. 26.1.1 - 26.1.4	
		"A PROM Element Based On Salicide Agglomeration Of Poly Fuses In A CMOS Logic Process"; Alavi et al.; 1997 IEEE; pp. 34.3.1 - 34.3.4	
		"Effects Of Thermal Processes After Silicidation On The Performance Of TiSi ₂ /Polysilicon Gate Device"; Jang et al.; IEEE Transactions On Electron Devices; Vol. 46; No. 12; December 1999; pp. 2353-2356	
		"Comparison Of Transformation To Low-Resistivity Phase And Agglomeration Of TiSi ₂ and CoSi ₂ "; Lasky et al.; IEEE Transaction On Electron Devices; Vol. 38; No. 2; February 1991; pp. 262-269	
		"CoSi ₂ Integrated Fuses On Poly Silicon For Low Voltage 0.18 um CMOS Application"; Kalnitsky et al.; 1999 IEEE; 4 pages	

Examiner Signature		Date Considered	
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